			25	m A

	Symbol			
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	42	
Continuous Drain Current (Package Limitec		T_C=25℃	35	
		-	120	V V
Pulsed Drain Current	I_{DM}	-	70	A
Avalanche Energy, Single Pulse				

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250 A	120	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 A	1.4	2.0	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=120V, T_j=25℃	-	-	1	A
		V_{GS}=0V, V_{DS}=120V, T_j=100℃	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=5A	-	20	25	m
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=5A	-	25	31	m
Transconductance	g_{fs}	V_{DS}=5V, I_D=5A	-	20	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	8.5	-	

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=60V, f=1MHz	-	977	-	pF
Output Capacitance	C_{oss}		-	143	-	
Reverse Transfer Capacitance	C_{rss}		-	6.2	-	
Total Gate Charge	Q_g(10V)	V_{DD}=60V, I_D=5A, V_{GS}=10V	-	13.5	-	nC
Total Gate Charge	Q_g(4.5V)		-	7.6	-	
Gate to Source Charge	Q_{gs}		-	2.8	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	2.0	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=60V, I_D=5A, V_{GS}=10V, R_G=10 ,	-	8	-	ns
Rise time	t_r		-	8	-	
Turn off Delay Time	$t_{d(off)}$		-	14	-	
Fall Time	t_f		-	9	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=60V, I_F=5A, dI_F/dt=500A/ s	-	25	-	ns
Reverse Recovery Charge	Q_{rr}		-	91	-	nC

Fig 1. Typical Output Characteristics

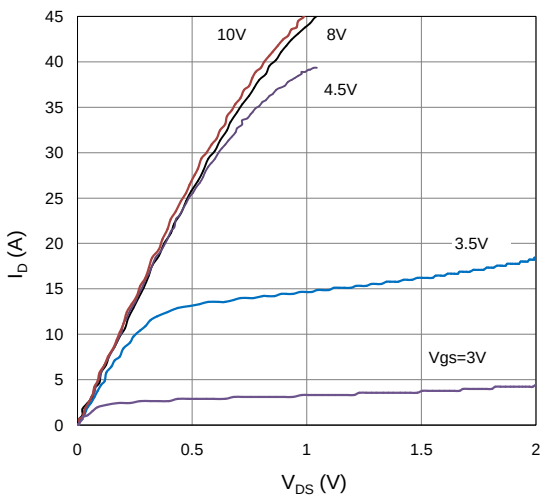


Figure 2. On-Resistance vs. Gate-Source Voltage

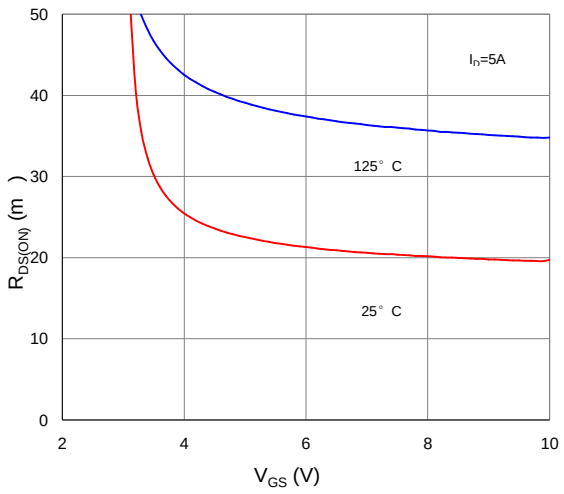


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

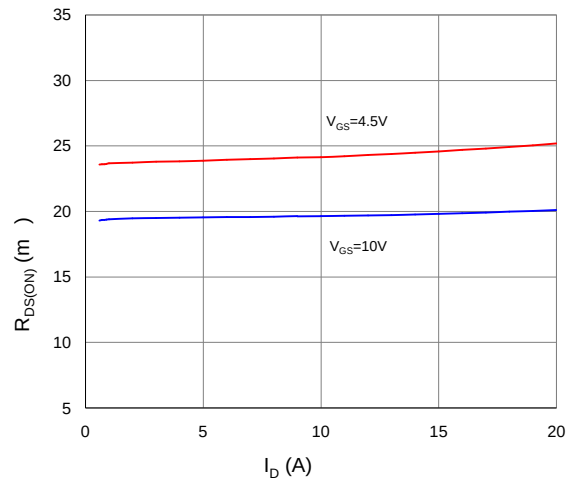


Figure 4. Normalized On-Resistance vs. Junction Temperature

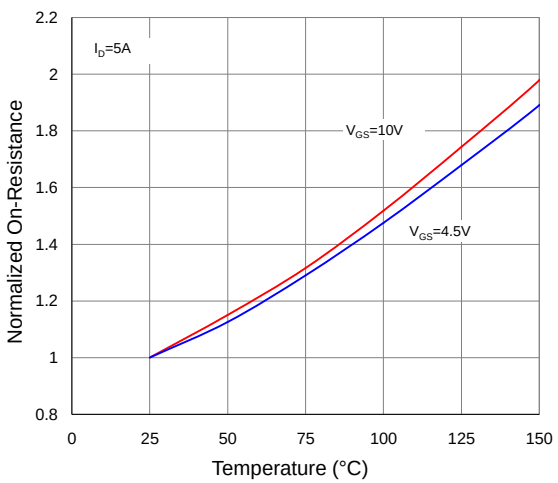


Figure 5. Typical Transfer Characteristics

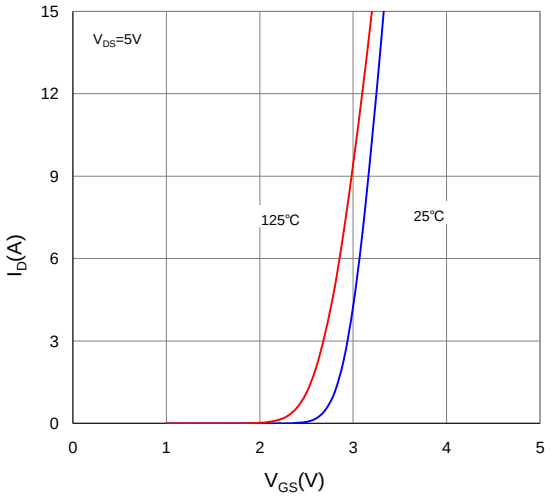


Figure 6. Typical Source-Drain Diode Forward Voltage

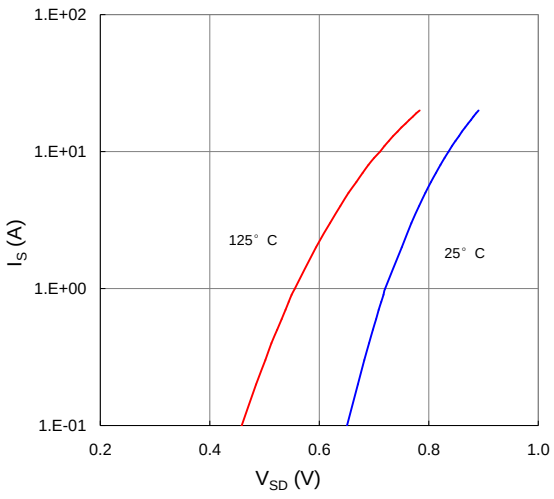


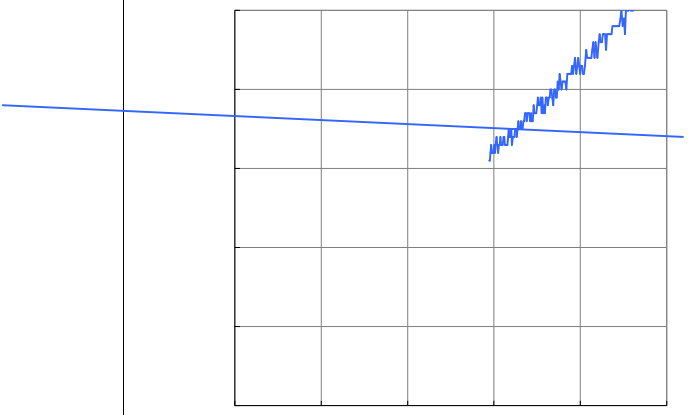
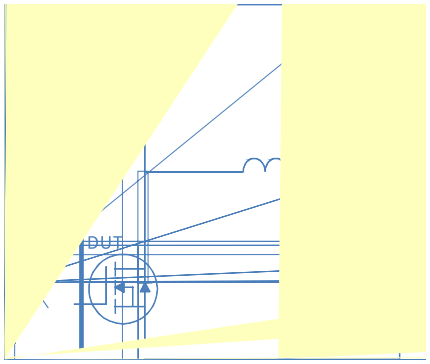
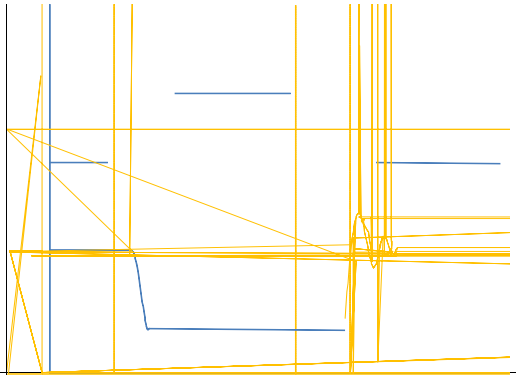
Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage	Figure 8. Typical Capacitance vs. Drain-to-Source Voltage
	

Figure 9. Maximum Safe Operating Area	Figure 10. Maximun Drain Current vs. Case Temperature
	A

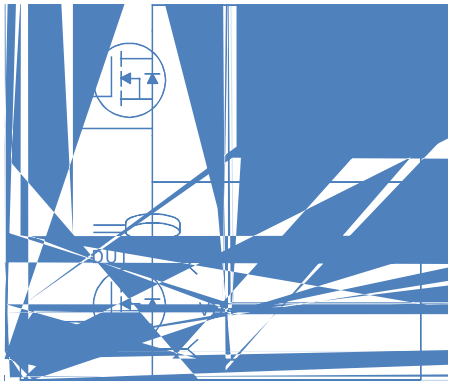
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

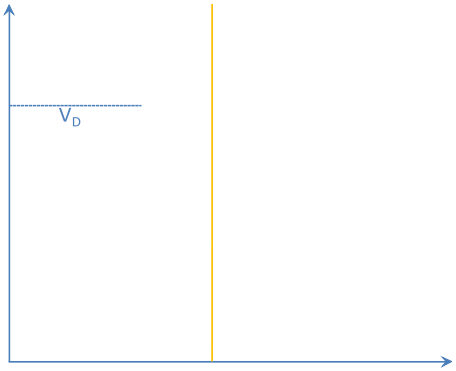
Inductive switching Test



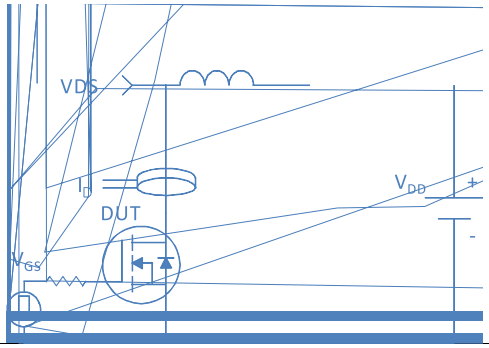


Gate Charge Test

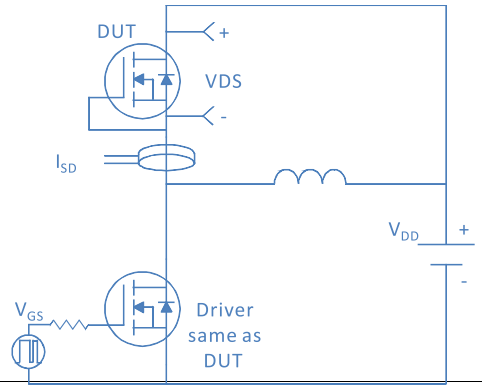


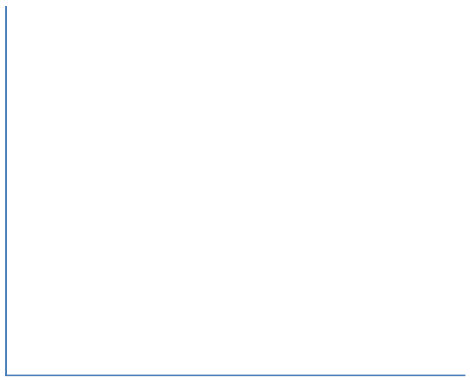


Uclamped Inductive Switching (UIS) Test



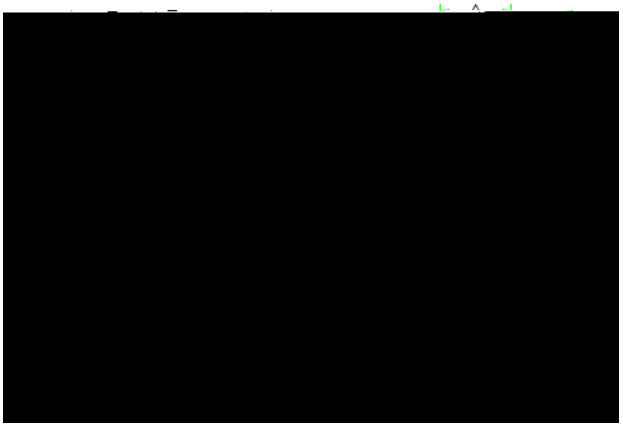
Diode Recovery Test





Package Outline

TO-252, 3 leads



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1		2.743 REF	
L2		0.508 BSC	
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223